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DATE MAILED: 01/17/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-47 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-47 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

Part III DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 10, 11, 14, 17, 18 and 33 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 10 and 11 line 1, the phrase "The overlay control circuitry" lacks clear and proper antecedent basis.

In claim 14 lines 8, 13-14 and 17-18, the phrase "and a word of data from said graphics pipeline otherwise" is vague and indefinite.

In claim 17 line 9 and 15, the phrase "control input" lack clear and proper antecedent basis. Are they first and second data inputs as per lines 3-4? And in lines 18-19 the phrases "said control input of said output selector" lacks clear and proper antecedent basis.

In claim 18 lines 2-3, the phrase "a third input coupled to a second output of said graphics pipeline" is vague and indefinite because claims 12 and 17, from which this claim depends, do not recite a first and second inputs and it is also not clear what is the second output of the graphics pipeline.

In claim 33 the phrase "said port" lacks clear and proper antecedent basis.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude

patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

3. Claims 1-6, 9-14, 17-21, 23, 26, 28 and 30-47 are rejected under 35 U.S.C. § 103 as being unpatentable over EDGE: Work-Group Computing Report, Oct. 3 1994, v5, n228, p15(1) (EDGE) and Jeff Mace "Mainstream graphics accelerators rush power" PC Magazine, Dec, 1994, v13, n21, p239 (17) (Mace).

As per claim 1, EDGE discloses that Cirrus Logic's MotionVideo Architecture includes a multi-format buffer that stores YUV signals from a video stream and RGB format from a computer (pg. 1) . EDGE does not expressly disclose writing data to on-screen and off-screen memory of the frame buffer. However on-screen and off-screen memories are well known and common in the art and Mace teaches using off-screen memory to change resolution and color depth of the video. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an on-screen and an off-screen area in the frame buffer to more efficiently use the memory space and so that the resolution and the color depth of the video can be changed as desired for better video display quality. EDGE also does not expressly disclose a graphics pipeline or a video pipeline. However since EDGE discloses graphics processing as well as video playback, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included graphics processing in a pipelined architecture for more efficient processing as well as a video

pipeline so that the stored video data may undergo processing such as scaling for resizing video-in-window more efficiently.

As per claims 2-4, EDGE does not disclose in a first mode, outputting graphics data, in a second mode, outputting video data when the display position corresponds to a particular display window, in a third mode, outputting video data based on the display position on the screen and when the graphics data match a color key, and in a fourth mode, outputting video data when the graphics data matches a color key. However it would have been obvious to select graphics or video data based on any combination of the display position on the screen and the color key match of the graphics data so that video data are displayed in an appropriate window at a desired location.

As per claim 5, EDGE does not expressly disclose maintaining a stream of graphics data to the graphics pipeline. However FIFOs are well known and common in the art for handling the differences in data rates. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a FIFO memory between the frame buffer and the graphics pipeline so that the difference in their data rates will still allow a stream of data to be provided to the graphics pipeline.

As per claim 6, EDGE discloses that there is a direct interconnect between a live television source and the computer enabling TV quality video. And since EDGE discloses storing both graphics and video data in the multi-format buffer, address generating circuitry is an inherent feature.

As per claims 9-11, EDGE does not expressly disclose counters, comparison circuitry, registers and logic gates for comparing. However, the use of these elements are well known and common in the art and therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use them to keep track of display position and locations of windows on the display and to

provide comparison results to satisfy particular conditions so that graphics and video data may be displayed in appropriate locations in appropriate windows.

As per claim 13, color look-up table in graphics processing is an inherent feature and EDGE discloses true-color video play-back.

As per claim 28, EDGE discloses video playback from a CD-ROM or a hard disk as well as a direct interconnect between a live television source and the computer.

As per claim 33, the use of dual-ported video memory is well known and common in the art and therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a dual-ported VRAM for the frame buffer so that data may be simultaneously read and written.

As per claim 38, EDGE discloses graphics processing as well as video playback but does not expressly disclose parallel graphics and video pipelines. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have included pipelined graphics processing as well as pipelined video processing in parallel for more efficient graphics and video processing.

Claim 12, 14, 17-21, 23, 26, 30-32, 34-37 and 39-47 are similar in scope to claims 1-11 and 33, and are rejected under the same rationale.

4. Claims 22, 24, 25 and 29 are rejected under 35 U.S.C. § 103 as being unpatentable over EDGE: Work-Group Computing Report, Oct. 3 1994, v5, n228, p15(1) (EDGE) and Jeff Mace "Mainstream graphics accelerators rush power" PC Magazine, Dec, 1994, v13, n21, p239 (17) (Mace) and Anthony Cataldo "WD, Cirrus show video playback ICs", Electronic News, Oct 1994, v40, n2035, p66(1) (Cataldo).

As per claim 22, EDGE does not expressly teach interpolation circuitry. However, Cataldo discloses a video playback controller comprising scaling, interpolation and chroma key features. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the

interpolation feature into the controller disclosed by EDGE so that it can be used for enlarging the video image for display.

As per claims 25 and 29, EDGE does not expressly disclose color conversion circuitry. However, Cataldo discloses logic for YUV to RGB color space conversion. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the color conversion of Cataldo in the systems disclosed by EDGE so that both video and graphics data may be stored in the same frame buffer.

Claim 24 is similar in scope to claim 22 and is rejected under the same rationale.

5. Claims 7, 8, 15, 16 and 27 are rejected under 35 U.S.C. § 103 as being unpatentable over EDGE: Work-Group Computing Report, Oct. 3 1994, v5, n228, p15(1) (EDGE) and Jeff Mace "Mainstream graphics accelerators rush power" PC Magazine, Dec, 1994, v13, n21, p239 (17) (Mace) and Dave Bursky "Acceleration puts the 'snap' into graphics", Electronic Design, July 1994, v42, n15, p55(9) (Bursky).

As per claims 7 and 8, EDGE does not expressly disclose first and second FIFOs for storing first and second display lines. However Bursky discloses a graphics accelerator that comprises FIFOs to compensate for data rate differences. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the FIFOs disclosed by Bursky in systems disclosed by EDGE so that two display lines may be stored in the FIFOs and so that additional processing such as interpolation of the two lines may be performed before display.

As per claim 27, Bursky discloses that the Power 9100 use a shared frame buffer architecture for storing both graphics and video and that it supports a packed pixel mode (pg. 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the packed pixel mode in the systems disclosed by EDGE to more efficiently store the data in memory.

Claims 15 and 16 are similar in scope to claims 7 and 8, and are rejected under the same rationale.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art deals with various graphics controllers.

James Turley "Brooktree reveals multimedia plans; new chip set merges audio, video, graphics on local bus" Microprocessor Report, Dec 1994, v8, n16, p19 (1).

Bill Snyder "The Cirrus seer" PC Week, Oct 1994, v11, n42, pA1(3).

Steve Undy et al. "A low-cost Graphics and Multimedia workstation chip set" IEEE Micro, April 1994, v14, issue 2, pgs 10-22.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. thru Fri. from 9:30 am to 3:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Powell, can be reached on (703) 305-9703. The fax phone number for this Group is (703) 308-5397.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Mark R. Powell
MARK R. POWELL
SUPERVISORY PATENT EXAMINER
ART UNIT 2415

ujc
January 3, 1996